



2116
EPW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 10/084,566

Filed: February 27, 2002

Inventor(s):
Madrid, et al.

Title: A METHOD AND
MECHANISM FOR
GENERATING A CLOCK
SIGNAL WITH A
RELATIVELY LINEAR
INCREASE OR
DECREASE IN CLOCK
FREQUENCY

§ Examiner: Patel, Nitin C.
§ Group/Art Unit: 2116
§ Atty. Dkt. No: 5500-80100
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I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

Rory D. Rankin

Printed Name

Signature

April 22, 2005

Date

RESPONSE TO OFFICE ACTION OF
MARCH 4, 2005

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This paper is submitted in response to the Office Action of March 4, 2005, to further highlight why the application is in condition for allowance.

Please amend the case as listed below.

IN THE TITLE

Please replace the title with the following new title:

-- A Method And Mechanism For Generating A Clock Signal With A Relatively Linear Increase Or Decrease In Clock Frequency--